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H03M 13/00 // H04L 9/00

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H4P PEP
U1S S2208 S2316

(56) Documents Cited

GB 2259226 A	GB 2071371 A	GB 2038144 A
GB 2019168 A	EP 0129223 A2	EP 0084913 A1
EP 0072640 A1	WO 82/03719 A1	US 4907233 A
US 4637021 A	US 4476562 A	

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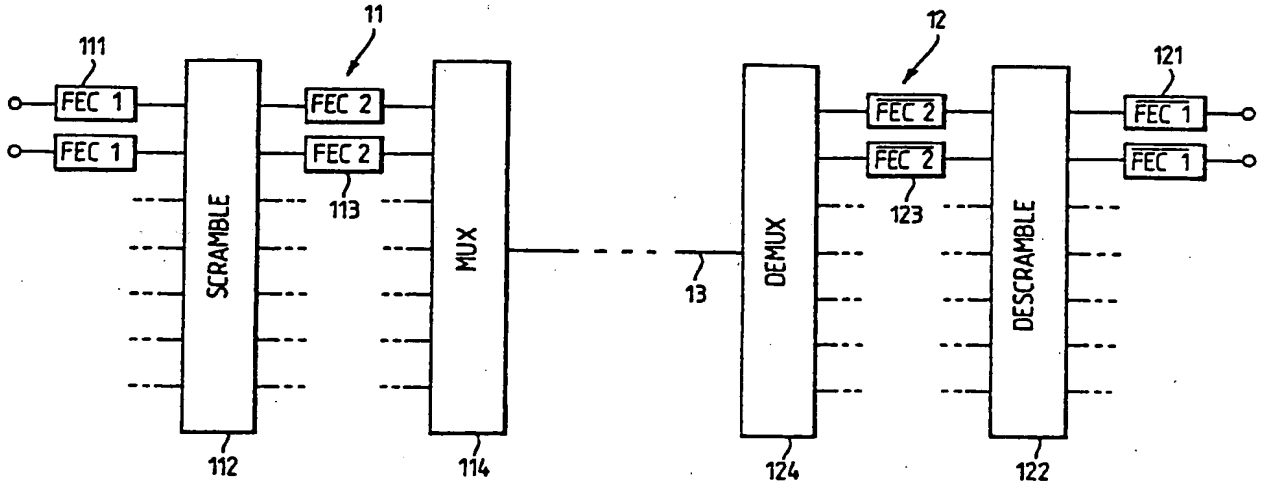
UK CL (Edition L) G4A AED , H4P PEL PEP PEX
INT CL^5 H03M 13/00

(54) **Digital transmission system with error correcting coding**

(57) A set of digital signals is transmitted over a potentially noisy channel 13 by effecting two stages of forward error correcting codes 111, 113 and two corresponding decoding stages 123, 121. The signal bits are interleaved or rearranged, e.g. by pseudorandom scrambling 112 between the first and second encoding and descrambling 122 between the first and second decoding. These redistribute transmission errors and improve the efficiency of the decoding process. Further, as the encoding is effected in two stages, relatively simple coder circuits may be employed.

Application is to optical transmission, e.g. submarine systems.

Fig. 1.



GB 2 275 393 A

At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

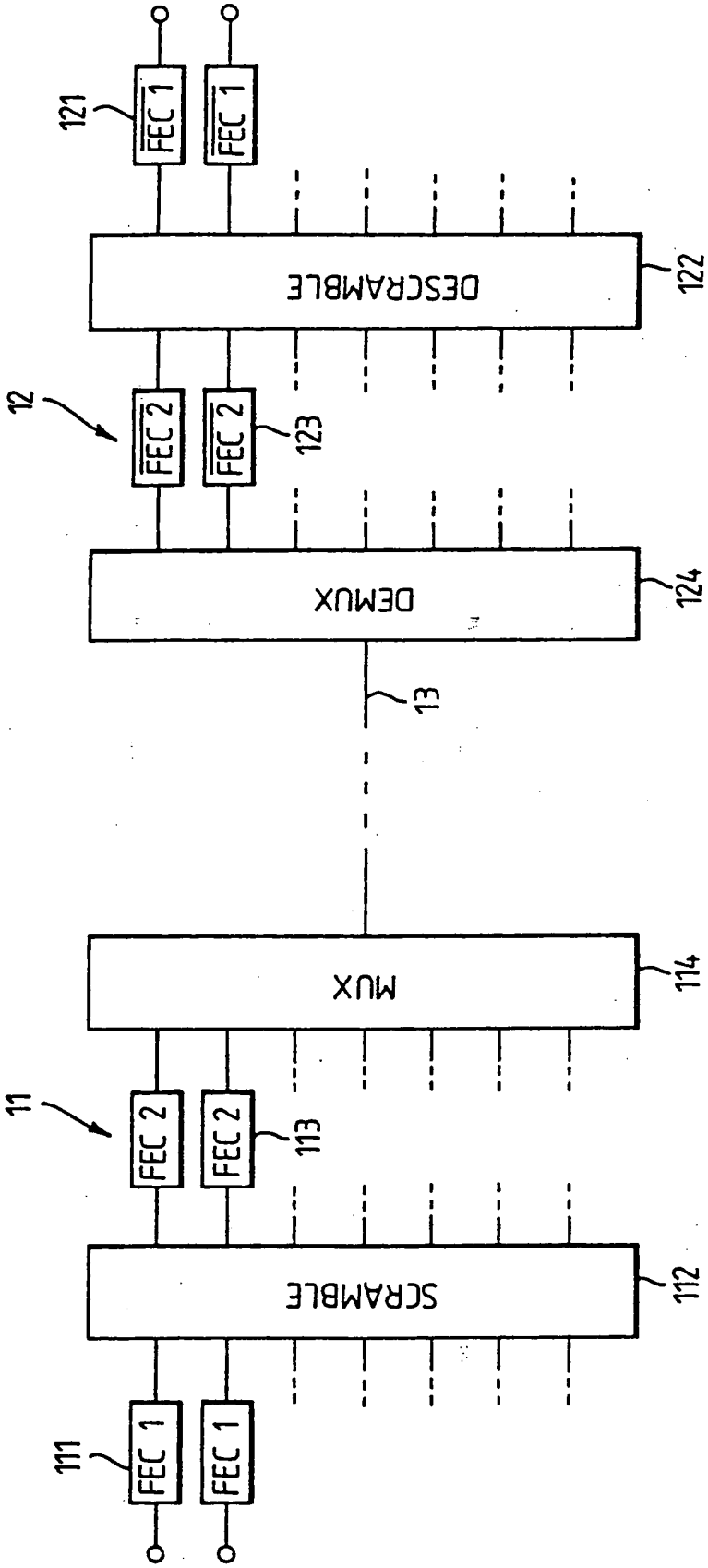

FEC 1
FEC 1
121
DESCRAMBLE
122
12
FEC 2
FEC 2
123
DEMUX
124
13
MUX
114
11
FEC 2
FEC 2
113
SCRAMBLE
112
111
FEC 1
FEC 1

Fig. 1.

Fig.2a

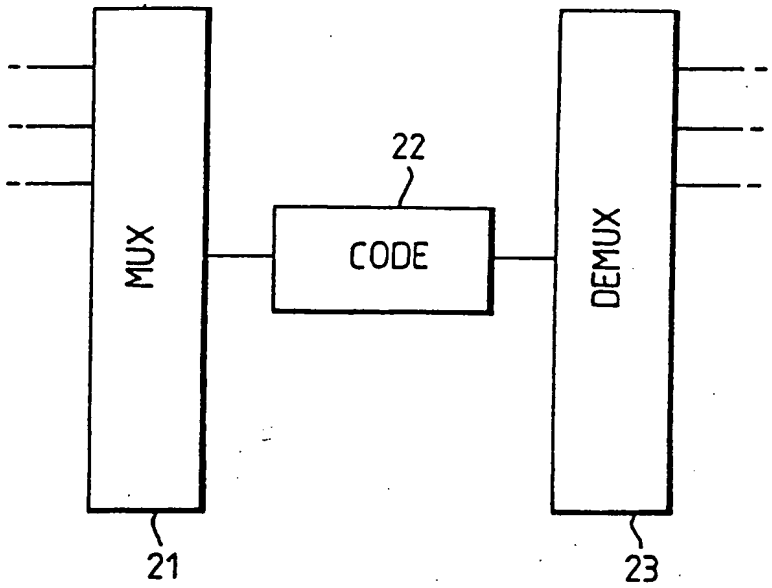


Fig.2b

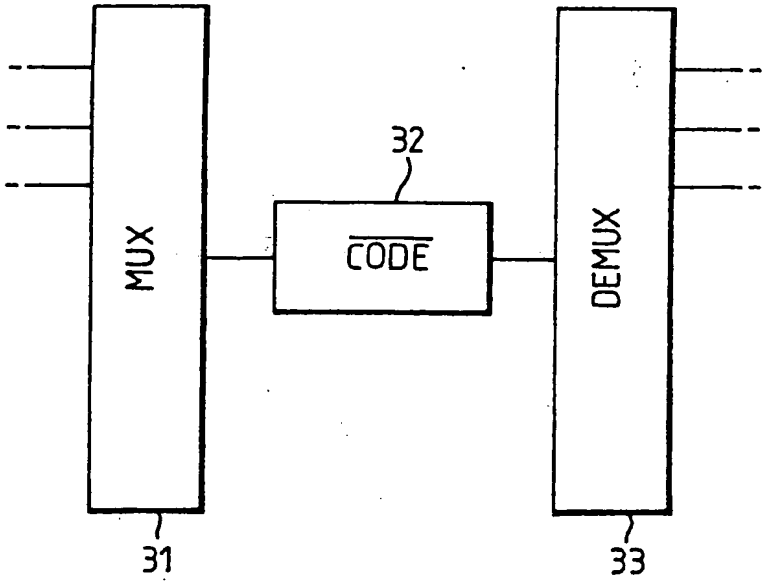
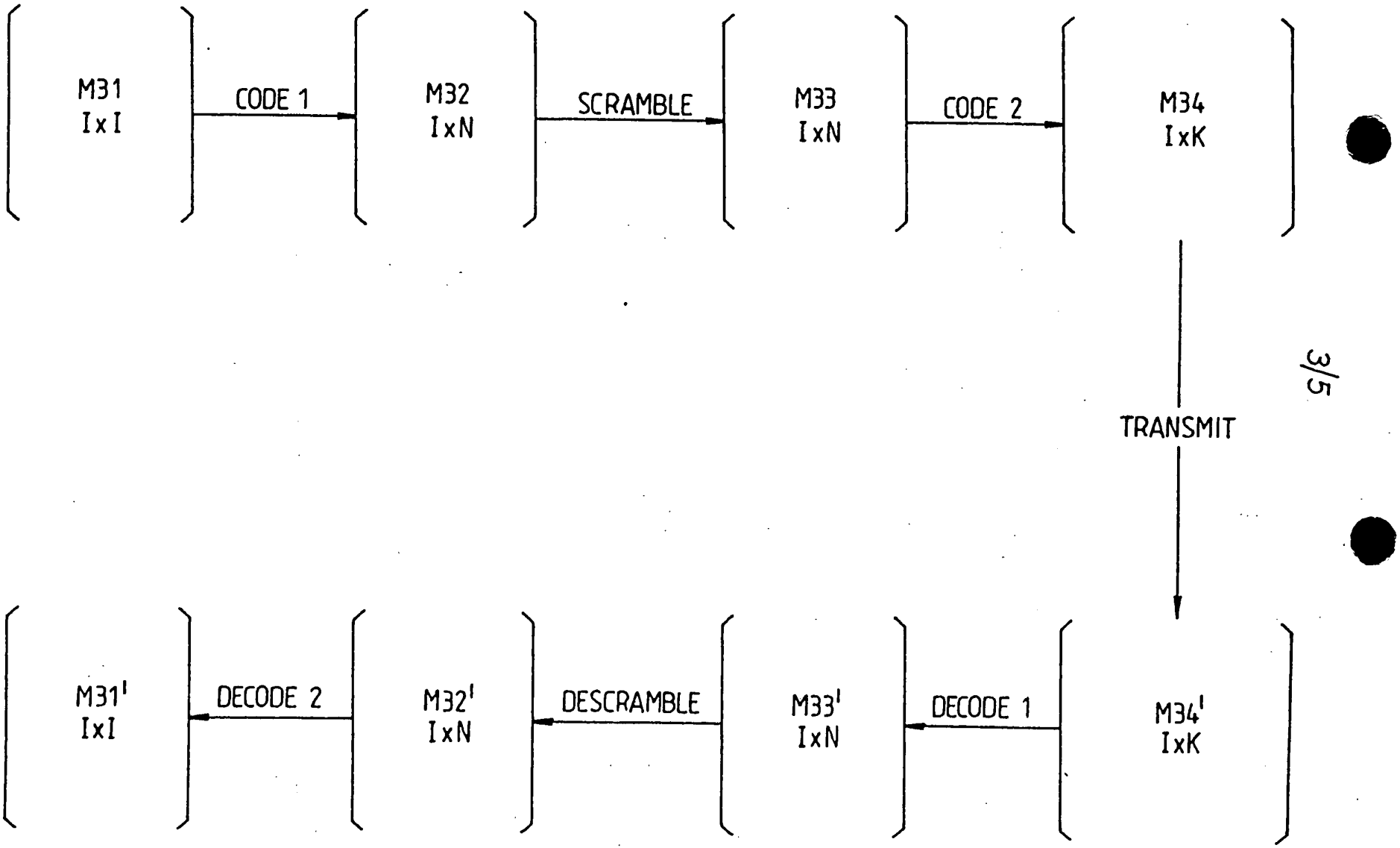


Fig.3.


M31
IxI
CODE 1
M32
IxN
SCRAMBLE
M33
IxN
CODE 2
M34
IxK
TRANSMIT
M31'
IxI
DECODE 2
M32'
IxN
DESCRAMBLE
M33'
IxN
DECODE 1
M34'
IxK

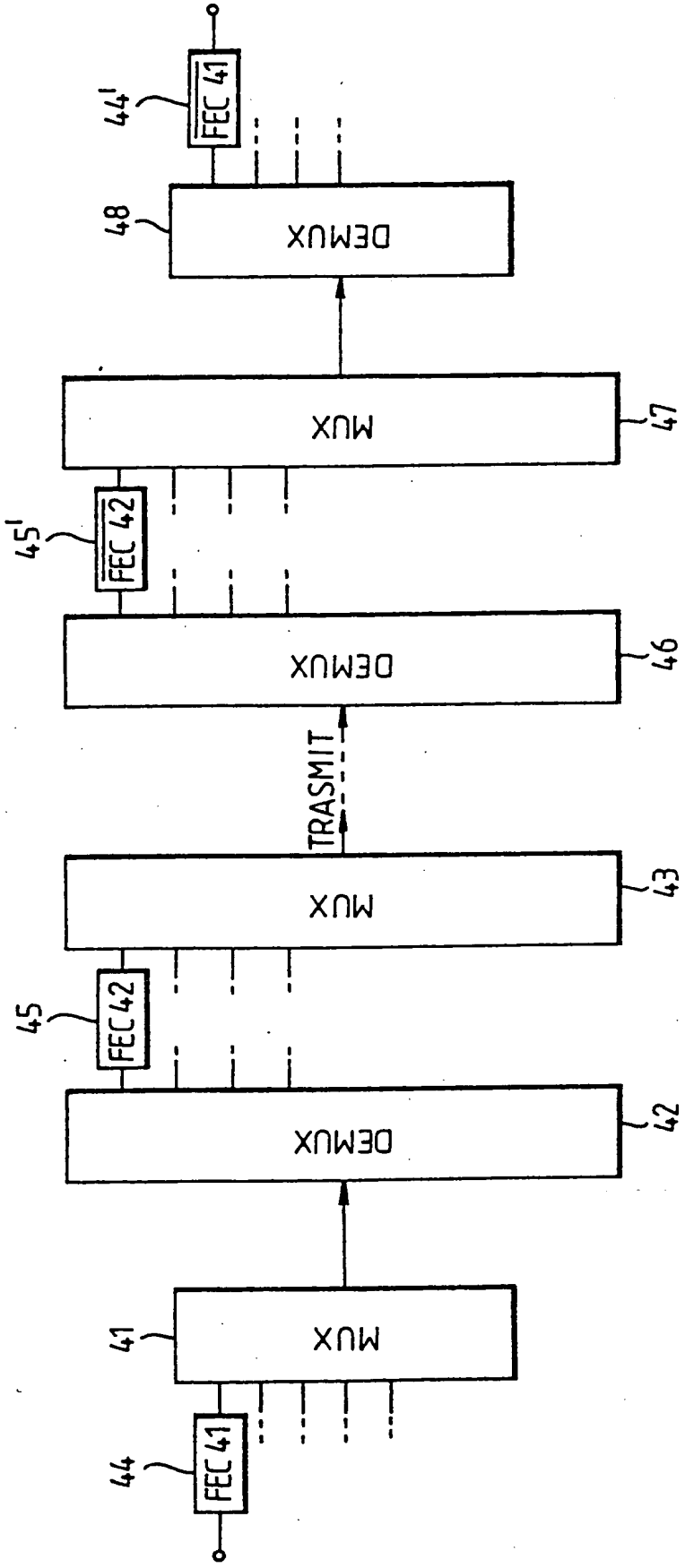
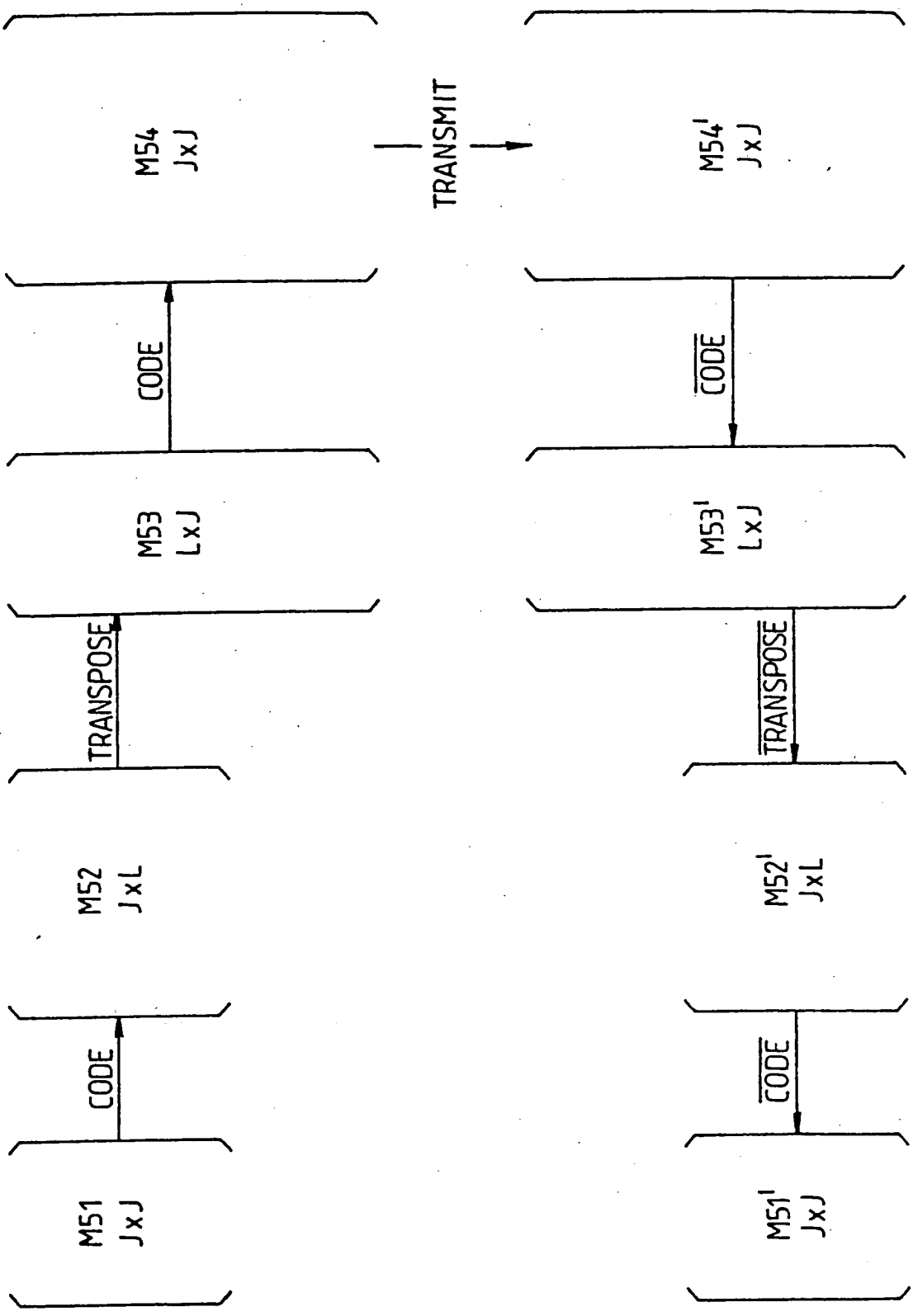

44'
FEC 41
48
DEMUX
MUX
47
45'
FEC 42
DEMUX
46
TRASMIT
MUX
43
45
FEC 42
DEMUX
42
41
MUX
44
FEC 41

Fig. 4.

Fig. 5.


M51
J x J
CODE
M52
J x L
TRANSPOSE
M53
L x J
CODE
M54
J x J
TRANSMIT
M51'
J x J
CODE
M52'
J x L
TRANSPOSE
M53'
L x J
CODE
M54'
J x J

TRANSMISSION SYSTEM

This invention relates to transmission systems, e.g. communications systems, in which signals are transmitted in a digital format, and in particular to error correction in such transmission systems.

Digital transmission systems transmit speech or data signals in the form of bit streams which represent a digital encodement of the information to be transmitted. A constant problem with techniques of this nature is the introduction of errors, e.g. missing bits or spurious bits, into the signal transmitted over the channel. Conventionally this problem is addressed by the use of error correcting coding techniques. One commonly used technique is block forward error coding (FEC). In this technique a rectangular, e.g. square block of J^2 information bits is encoded into a corresponding block of N^2 bits, where $N > J$, for transmission over the channel. At the receiver the block of N^2 bits is decoded to recover the original block of J^2 bits. The block code is designed to permit correction of errors that may arise over the transmission path. Such a system is described for example in specification No. EP-B1-157413.

It is assumed that x errors are introduced to the encoded block of N^2 bits over the transmission path where x varies randomly from block to block. The mean value of x is related inter alia to the noise level of the channel; the particular code employed will be designed to take account of the value of x and of the anticipated

statistical variation in that value. In general, block forward error correcting codes can correct fully for up to C errors per block where C is a function of the block size N^2. Typically the value of C is determined from the condition that

$$\frac{2^N}{2^J} \geqslant 1 + N + \frac{N(N-1)}{2} + \ldots \qquad C+1 \text{ terms)}$$

If $x \leq C$ then the block is received error free, but if $x > C$ then there is no error connection at all and X errors are received (in some codes the number of errors is increased and 2x errors are received).

A key factor in the design of an error correcting code is the coding gain. This is defined as a measure of the change in signal to noise ratio achieved by application of the code and increases with the value of N. Thus, for relatively noise free transmission it is desirable for N to be large. However, as the block size N^2 increases, the complexity of the coding and decoding algorithms increases very rapidly. This places great demands on the design of the integrated circuit chips that are employed to perform the coding and decoding process and imposes a heavy computational load on the transmission system..

The object of the invention is to minimise or to overcome this disadvantage.

According to the invention there is provided a method of transmitting a set or block of digital signal elements or bits over a potentially noisy channel, the method including applying first and second forward error correcting codes to the set of bits, transmitting the encoded bits, and applying first and second forward error decoding of the encoded bits to recover the set of signals, and wherein the signal bits of said set are rearranged between said first and second encodings and between said first and second decodings whereby to redistribute errors in the set of signal bits.

According to another aspect of the invention there is provided apparatus for transmitting a set or block of digital signals over a potentially noisy channel, the apparatus including means for effecting a first forward error correction coding of the signal, means for rearranging the bits of the encoded signals, means for effecting a second forward error correction coding of the rearranged signals, means for transmitting the encoded rearranged signals over the channel, means for effecting a first decoding of the signals transmitted over the channel whereby to correct at least some transmission errors, means for rearranging the bits of the decoded signals whereby to redistribute uncorrected transmission errors, and means for effecting a second decoding of said rearranged signals whereby to correct substantially all remaining errors and recover the set of digital signals.

Embodiments of the invention will now be described with reference to the accompanying drawings in which:-

Fig. 1 is a schematic design of a multiplex transmission system incorporating two stages forward error coding at the tributary level;

Figs. 2a and 2b illustrate respectively a descrambler and a descrambler arrangement for use in the transmission system of Fig. 1;

Fig. 3 illustrates the error correcting coding and decoding process used in the system of Fig. 1;

Fig. 4 illustrates an alternative transmission system; and

Fig. 5 illustrates the error coding and decoding process associated with the system of Fig. 4.

Referring to Fig. 1, the transmission system includes a transmitter circuit 11 to which a number, typically sixteen, of tributaries are fed, a receiver circuit 12 having outputs corresponding to the number of input tributaries, and a transmission path 13 therebetween. The transmission path may comprise e.g. an optical

fibre path or a radio link. Each input and output tributary carries a signal in the form of a bit stream.

The transmission circuit 11 incorporates a scrambler 112 having inputs and outputs equal in number to the number of tributaries. Each scrambler input is provided with a forward error correcting order circuit (FEC1) 114 which applies a first error correcting code to successive strings of I input signal bits to provide a corresponding stream of N encoded bits which stream is fed to the corresponding input of the scrambler 112.

The scrambler 112 interleaves the bits of its I input signals so that the N bits of each input signal are distributed evenly among the scrambler outputs which thus comprise I signals each of bit length N and each comprising bits from each of the input bit streams.

The I outputs of the scrambler 112 are fed each to a corresponding second forward error correcting coder circuits (FEC2) 113, which circuit applies a second error correcting code to the N-bit signal to provide a corresponding output signal of bit length K where $K > N$.

The outputs from the second forward error correcting circuits 113 are fed each to the corresponding input of a multiplexer 114 for transmission as a single, e.g. time division multiplexed signal over the transmission path 13 to the receiver 12. It will be appreciated that noise in the transmission path may corrupt some of the transmitted bits of the multiplexed signal thus introducing errors. The purpose of the error correcting coding applied to the signal is to negate or minimise the effects of those errors.

The receiver 12 comprises a demultiplexer 124 having I outputs corresponding to the I inputs of the multiplexer 114 and each provided with a second forward error decoder circuit $\overline{\text{(FEC2)}}$ 123 which circuit performs an inverse algorithm corresponding to the

second coder circuit 113. Each K-bit signal for the demultiplexer 124 is thus decoded to a corresponding N-bit signal which is then fed to the corresponding input of a descrambler 122.

The descrambler disinterleaves the bits of the N-bit signals applied to its I inputs to recover the I coded N-bit signals corresponding to the coded signals at the inputs of the scrambler 112. Each descrambled signal is then fed to a corresponding first forward error decoder circuit $\overline{(FEC1)}$ 124 which applies to that signal the inverse algorithm corresponding to the coder circuit 114. This process recovers the original I signals each of bit length L.

The construction of the scrambler and that of the descrambler are illustrated in Fig. 2a and Fig. 2b respectively. Referring first to Fig. 2a, the scrambler 112 comprises an input multiplexer 21 whose single output is fed via a pseudo-random coder 22 to an output demultiplexer 23 having a plurality of outputs. As previously described with reference to Fig. 1, the outputs of the demultiplexer 23 are fed each via a respective second forward error correcting circuit to the multiplexer 113 (Fig. 1) for transmission in multiplexed form over the transmission channel to the receiver end of the system.

The descrambler 122 is shown in Fig. 2b and comprises an input multiplexer 31 having a plurality of inputs corresponding to the outputs of the demultiplexer 123 (Fig. 1). The multiplexer 31 has a single output feeding a decoder 32 whose key corresponds to the pseudo-random code of the coder 22 of Fig. 2a. The output of the decoder is fed to an output demultiplexer 33 having outputs corresponding to the input tributaries of the descrambler 112 (Fig. 1).

Fig. 3 illustrates the operation of the forward error coding and decoding process employed in the arrangement of Fig. 1. The set of I-bit input signals applied to the inputs of the transmitter of Fig. 1

can be considered comprising the elements of an IxI matrix (M31) each element being a binary one or zero. The first coding stage operates on the rows of this matrix to form an IxN (I rows and N columns) matrix 32. The elements of this matrix are then scrambled to form a new IxN matrix M33. The second encodement step is then performed on the rows of this matrix to form a further IxK matrix M34 which represents the information that is transmitted over the transmission path.

During transmission errors are introduced to the signal so that the received matrix M34' differs from the transmitted matrix M34 in respect of those elements where an error has occurred. These errors comprise replacement of a binary one by a zero and vice versa. The errors are substantially corrected by the decoding process.

The received IxK signal matrix M34' is subjected to the second forward error decoding step, i.e. the inverse of the second forward error coding step to provide a decoded IxN matrix M33'. This decoding step decodes the rows of the matrix M34' and, where the number of errors in any one row is not excessive, corrects those errors. If however a row of the matrix M34' contains more errors than can be corrected by the decoding algorithm, then those errors will remain in the corresponding row of the decoder matrix M33'.

The signal matrix M33' is subjected to descrambling to generate a further IxN matrix M32'. The effect of the descrambling process is to redistribute the elements, including the errors, of the matrix M33' so that where a row of that matrix contained an excessive number of errors, those errors will now be substantially uniformly distributed amongst the rows of the descrambled matrix M32'. The next decoding stage decodes the rows of the matrix M32' to correct most if not all of those remaining errors to obtain the desired IxI output signal matrix M31'.

The technique provides in effect two stages of parallel stream encryption and two corresponding stages of parallel stream

decryption, these being a redistribution of the signal, and thus of the errors between the two stages of decryption.

Referring now to Fig. 4, this shows an alternative transmission system. Fig. 5 illustrates the matrix transformations associated with the system of Fig. 4.

The transmitter of Fig. 4 comprises an input multiplexer 41 coupled via a demultiplexer 42 to an output multiplexer 43. The input multiplexer 41 has a plurality J of inputs or tributaries corresponding to the number of input signals and each provided with a first forward error correcting circuit (FEC. 1) 44. Conveniently each input signal is of bit length J so that the input signal bits can be regarded as the elements of a JxJ matrix M51 (Fig. 5). Each first forward error correcting code circuit 44 encodes the corresponding J-bit input signal into a corresponding encoded signal of length L bits. The input to the input multiplexer 41 thus comprises a JxL matrix M52.

The input multiplexer interleaves the bits of its input signals into a single output which is fed to the demultiplexer 42.

The demultiplexer 42 has a plurality of outputs equal in number to the number L of columns of the matrix M52 and among which the bits of the demultiplexed signal are evenly distributed in the form of J-bit signal streams. The effect of the multiplexing and demultiplexing of the signal is to transpose the rows and columns of the JxL matrix 52 to form an LxJ matrix M53.

The J-bit length signals representing the rows of this matrix M53, i.e. each output of the demultiplexer 42, are encoded each by a respective second forward error correcting coding circuit (FEC42) 45. The first and second forward error correcting coding circuits operate on bits streams of the same length J and thus may conveniently employ the same encodement algorithm.

The doubly encoded signals comprising the rows of the matrix M53 are fed to the corresponding inputs of the output multiplexer 43 which, interleaves the signal bits into a single multiplexer signal for transmission to the receiver station.

As can be seen from Fig. 4 the construction of the receiver is the inverse of that of the transmitter. The receiver comprises an input demultiplexer 46, a multiplexer 47 and an output demultiplexer 48.

As described above with reference to Fig. 1, the transmitted multiplexed signal is subject to error introduced in the transmission path. Thus, the received signal, after demultiplexing by the input demultiplexer 46 comprises a LxJ matrix M54' identical to the matrix M54 apart from those elements which now constitute errors.

Some of the errors in the matrix M54' are corrected by passing the signals corresponding to the rows of the matrix each through a corresponding second forward error decoder circuit (FEC42) 451. This process transfers the received KxK matrix M54' to the partially decoded KxJ matrix M53'.

The K J-bit signals corresponding to the rows of the matrix M53' are fed to the K inputs of the multiplexer 47 whose single output is fed to the output demultiplexer 48.

The multiplexer 47 and the output demultiplexer 48 together perform the inverse transposition of the input multiplexer 41 and the demultiplexer 42, i.e. the rows and columns of the LxJ matrix M53' are transposed to form the JxL matrix 52'. This matrix corresponds to the matrix M52 but contains those errors still remaining after one stage of the error decoding process. It will be appreciated that, as a result of this transposition, that a plurality of errors remaining in any one row of the matrix M53' will be distributed amongst the rows of the transposed matrix M52'. This

minimises the effect of the remaining errors on the next decoding step effected via decoder $\overline{(FEC41)}$ 441 which applies the inverse algorithm to that of the coder 45. The decoding step removes all, or substantially all, of the remaining errors to recover the required JxJ signal matrix 51' which is identical with, or substantially identified with, the original input signal matrix M51.

It will be appreciated that in the system of Fig. 4, each stage of encodement requires an algorithm which generates only N bits. This can be compared with a conventional single stage encodement technique which requires an algorithm adapted to generate blocks of N^2 bits. The present technique thus represents a considerable saving in the computational load required for the encodement process and allows the use of relatively simple, and thus low cost, integrated circuit chips to perform the encodement and decodement.

The technique described above is of particular application to optical transmission systems, e.g. submarine systems. It is not however limited to this application and may also be employed e.g. in free space transmission systems. In the latter application the scrambling of the transmitted signal can provide effective security against eavesdropping by third parties.

CLAIMS:

1. A method of transmitting a set or block of digital signal elements or bits over a potentially noisy channel, the method including applying first and second forward error correcting codes to the set of bits, transmitting the encoded bits, and applying first and second forward error decoding of the encoded bits to recover the set of signals, and wherein the signal bits of said set are rearranged between said first and second encodings and between said first and second decodings whereby to redistribute errors in the set of signal bits.

2. A method of transmitting a plurality of digital signals in parallel over a potentially noisy transmission path, the method including encoding each said signal with a first forward error correcting code, rearranging the bits of the encoded signals to provide a new set of signals, encoding said new signals each with a further forward error correcting code, transmitting the rearranged encoded signals over the transmission path, applying a first decoding to the signals received over the transmission path whereby to correct at least some errors introduced to the signals during transmission, rearranging the bits of the decoded signals to provide a further set of signals and whereby to redistribute remaining uncorrected errors among the signals of said set, and further decoding said further set of signals whereby to correct substantially all the remaining errors and recover said plurality of digital signals.

3. A method of transmitting over a potentially noisy channel a plurality or set of digital signals each of the same bit length, the method including applying a first error correcting code to each said digital signal to provide a respective first encoded signal, rearranging or interleaving the bits of the first encoded signal whereby to obtain a second set of encoded signals, applying a second error correcting code to each signal of the second set whereby to obtain a respective doubly encoded signal, transmitting the doubly encoded signal over a transmission path, effecting a first decoding of the doubly encoded

signal whereby to recover the second set of encoded signals and to correct at least some transmission errors, rearranging or disinterleaving the bits of the second set of signals whereby to recover the first encoded signals and to redistribute remaining transmission errors among the bits of the second set, and effecting a second decoding of the rearranged signals whereby to remove substantially all remaining errors and recover said plurality of digital signals.

4. A method as claimed in claim 3, wherein said interleaving and disinterleaving of the said bits comprises pseudorandom scrambling and descrambling respectively.

5. A method of signal transmission substantially as described herein with reference to Figs. 1 to 3 or to Figs. 1, 4 and 5 of the accompanying drawings.

6. Apparatus for transmitting a set or block of digital signals over a potentially noisy channel, the apparatus including means for effecting a first forward error correction coding of the signal, means for rearranging the bits of the encoded signals, means for effecting a second forward error correction coding of the rearranged signals, means for transmitting the encoded rearranged signals over the channel, means for effecting a first decoding of the signal transmitted over the channel whereby to correct at least some transmission errors, means for rearranging the bits of the decoded signals whereby to redistribute uncorrected transmission errors, and means foe effecting a second decoding of said rearranged signals whereby to correct substantially all remaining transmission errors and recover the set of digital signals.

7. Apparatus for transmitting a set of digital signals substantially as described herein with reference to and as shown in Figs. 1 to 3 or Figs. 1, 4 and 5 of the accompanying drawings.

Patents Act 1977
Examiner's report to the Comptroller under Section 17 (The Search Report) - 12 -

Application number
[redacted]9303450.2

Relevant Technical fields

(i) UK Cl (Edition L) H4P (PEL, PEP, PEX); G4A (AED)

(ii) Int Cl (Edition 5) H03M 13/00

Search Examiner
K WILLIAMS

Databases (see over)
(i) UK Patent Office

(ii)

Date of Search
12 APRIL 1993

Documents considered relevant following a search in respect of claims 1-4 AND 6

Category (see over)	Identity of document and relevant passages		Relevant to claim(s)
X,E	GB 2259226 A	(RACAL-SES) 3 March 1993 See Figures 1 and 2	1, 2, 3, 6
X	GB 2071371 A	(SONY) See page 6, lines 15-30	1, 2, 3, 6
X	GB 2038144 A	(SONY) See whole specification	1, 2, 3, 6
X	GB 2019168 A	(SONY) See pae 5, lines 48-54	1, 2, 3, 6
X	EP 0129223 A2	(HITACHI) See Claim 5	1, 2, 3, 6
X	EP 0084913 A1	(PHILIPS) See abstract	1, 2, 3, 6
X	EP 0072640 A1	(SONY) See abstract	1, 2, 3, 6
X	WO 82/03719 A1	(SONY) See abstract	1, 2, 3, 6
X	US 4907233	(NASA) See abstract; Figure 1	1, 2, 3, 6
X	US 4637021	(PIONEER) See column 2, line 45 - column 3, line 23	1, 2, 3, 6

		to claim(s)

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Examiner's report to the Comptroller under Section 17 (The Search Report) — 14 —

Application number
[redacted]9303450.2

Relevant Technical fields

(i) UK Cl (Edition) Contd. from page 2

(ii) Int Cl (Edition)

Search Examiner

K WILLIAMS

Databases (see over)

(i) UK Patent Office

(ii)

Date of Search

12 APRIL 1993

Documents considered relevant following a search in respect of claims

Category (see over)	Identity of document and relevant passages		Relevant to claim(s)
X	US 4476562	(SONY) See column 1, lines 21-52; see column 12 line 16 to column 13, line 5	1, 2, 3, 6

Category	Identity of document and relevant passages	Relevant to claim(s)

Categories of documents

X: Document indicating lack of novelty or of inventive step.

Y: Document indicating lack of inventive step if combined with one or more other documents of the same category.

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&: Member of the same patent family, corresponding document.

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